

FIG.1 PRIOR ART

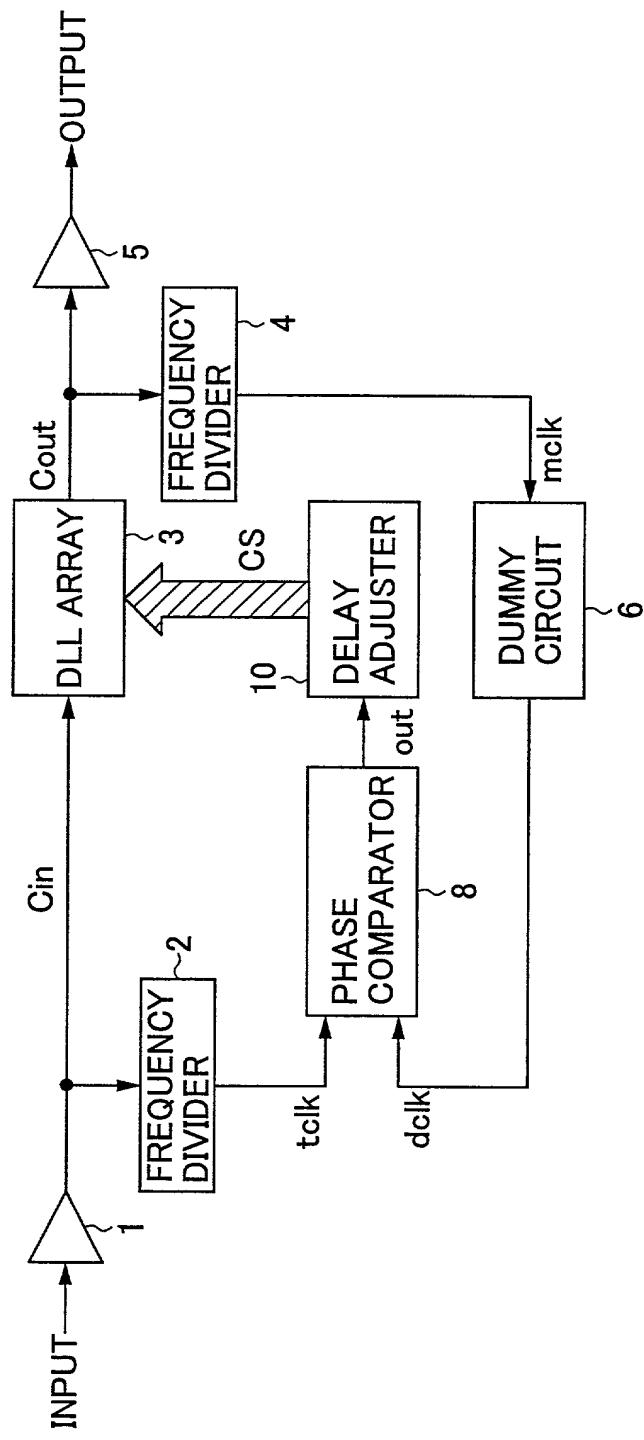
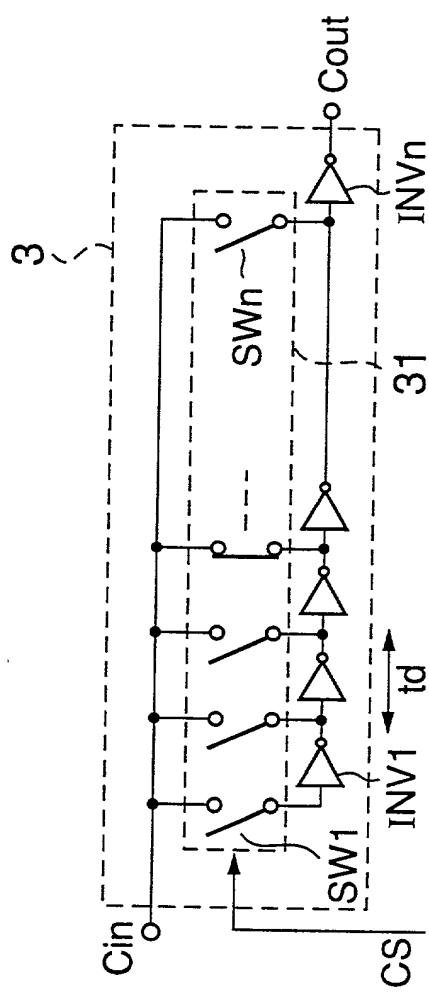


FIG. 2 PRIOR ART



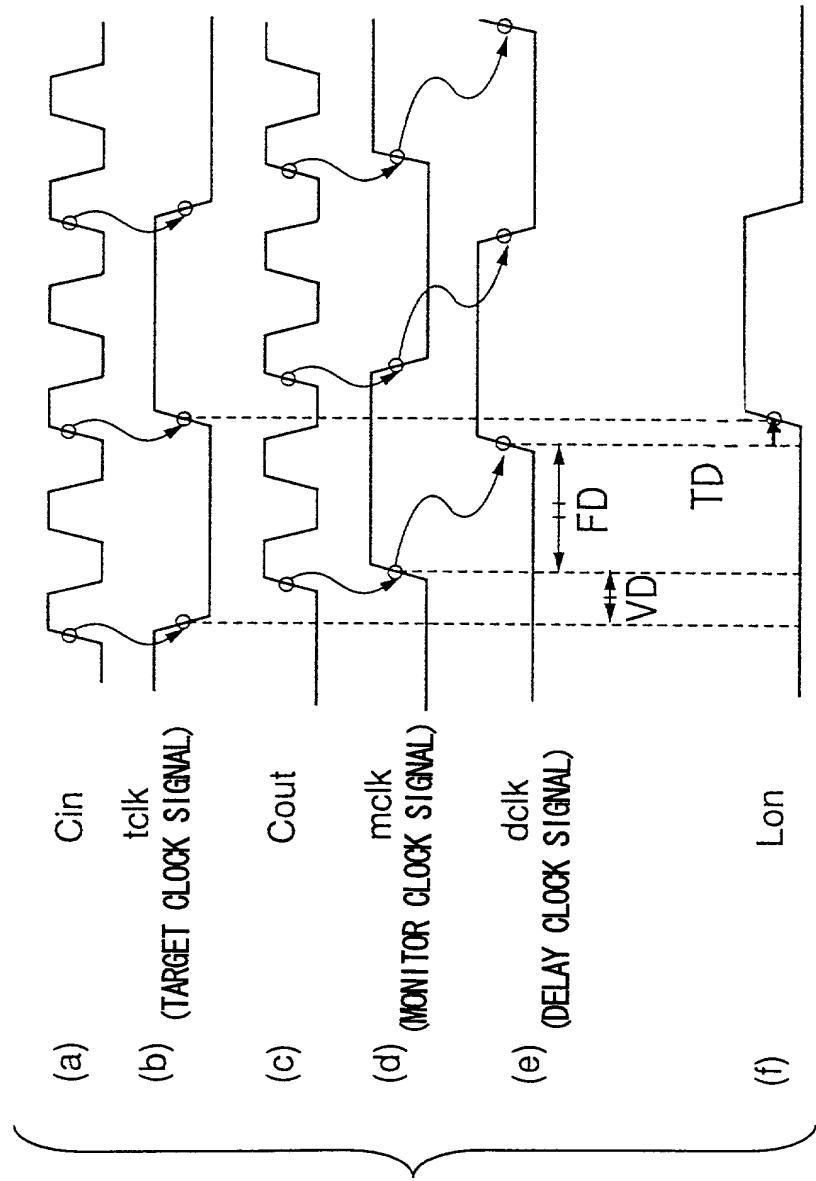


FIG. 3
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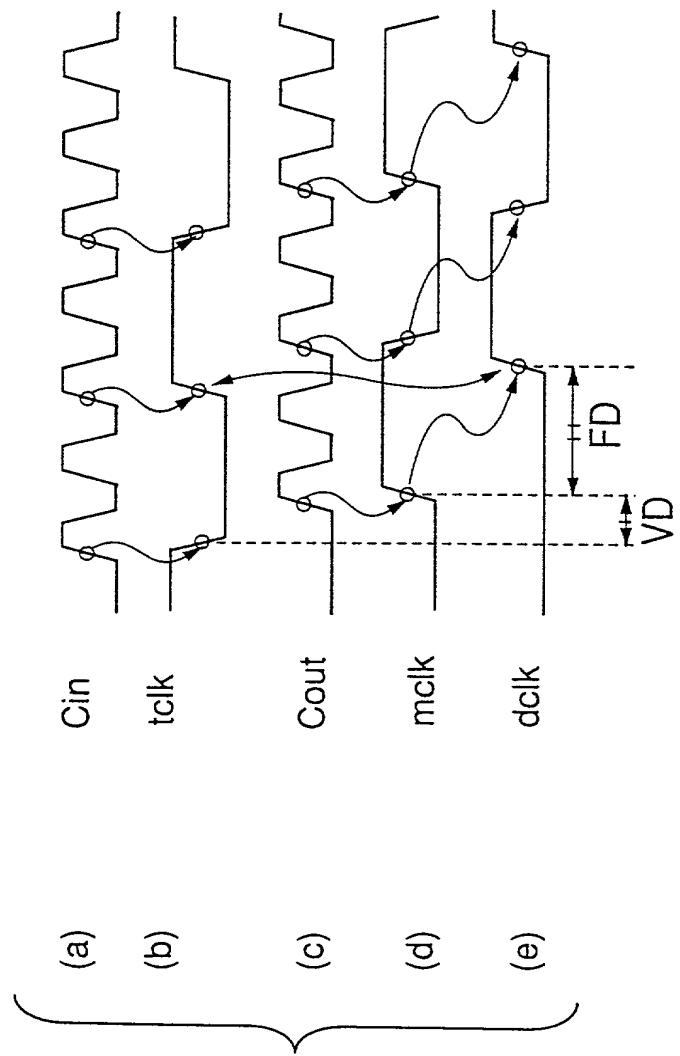
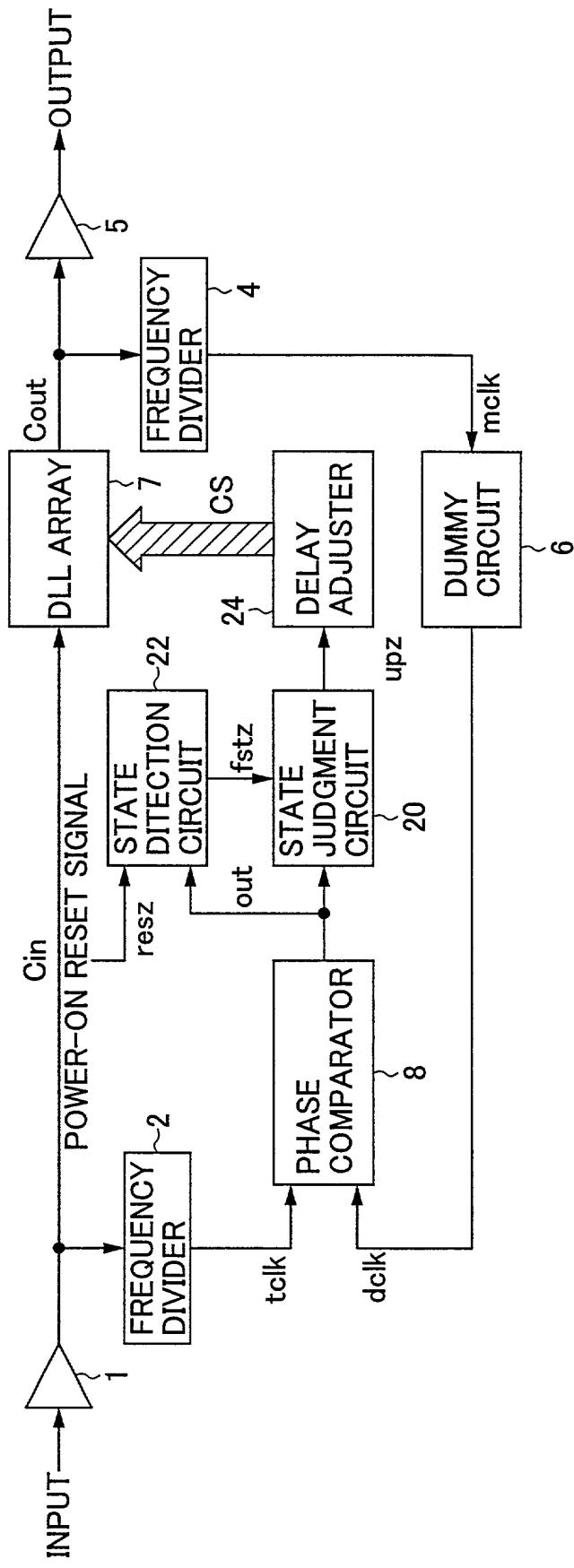


FIG. 4
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FIG.5



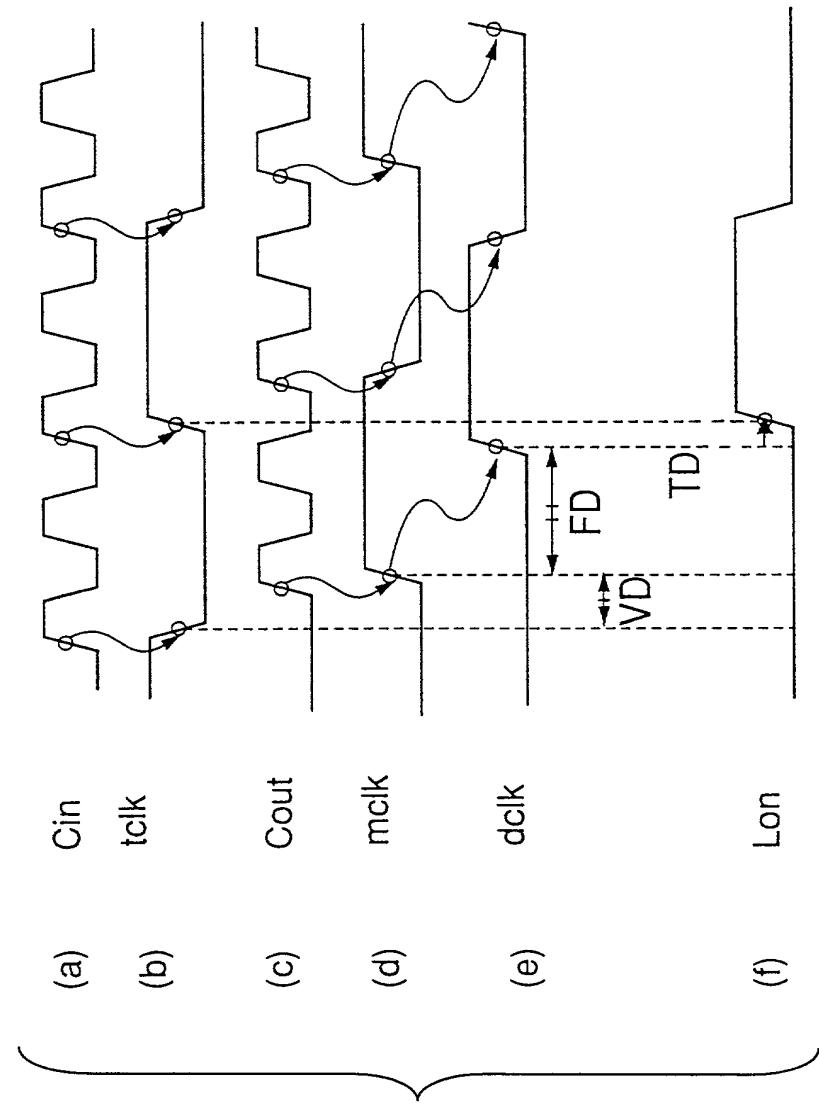


FIG. 6

Figure 7: A diagram illustrating a digital circuit structure, likely a memory or register file, showing data flow and timing. The circuit consists of six stages (a-f) connected in series. Stage (a) is an input stage with a Cin input and a tclk control signal. Stage (b) is a first data stage with a Cin input and a tclk control signal. Stage (c) is a second data stage with a Cin input and a tclk control signal. Stage (d) is a third data stage with a Cin input and a tclk control signal. Stage (e) is a fourth data stage with a Cin input and a tclk control signal. Stage (f) is an output stage with a Lon output. The circuit uses a multi-bit bus structure, indicated by the multiple lines for Cin and tclk. The Lon output is shown as a single line. The circuit is synchronized by a shared mclk signal. The timing diagram on the right shows the relationship between the mclk signal, the data stages (FD, VD, AD), and the final output Lon. The diagram indicates that the data is read out during the AD phase of the clock cycle.

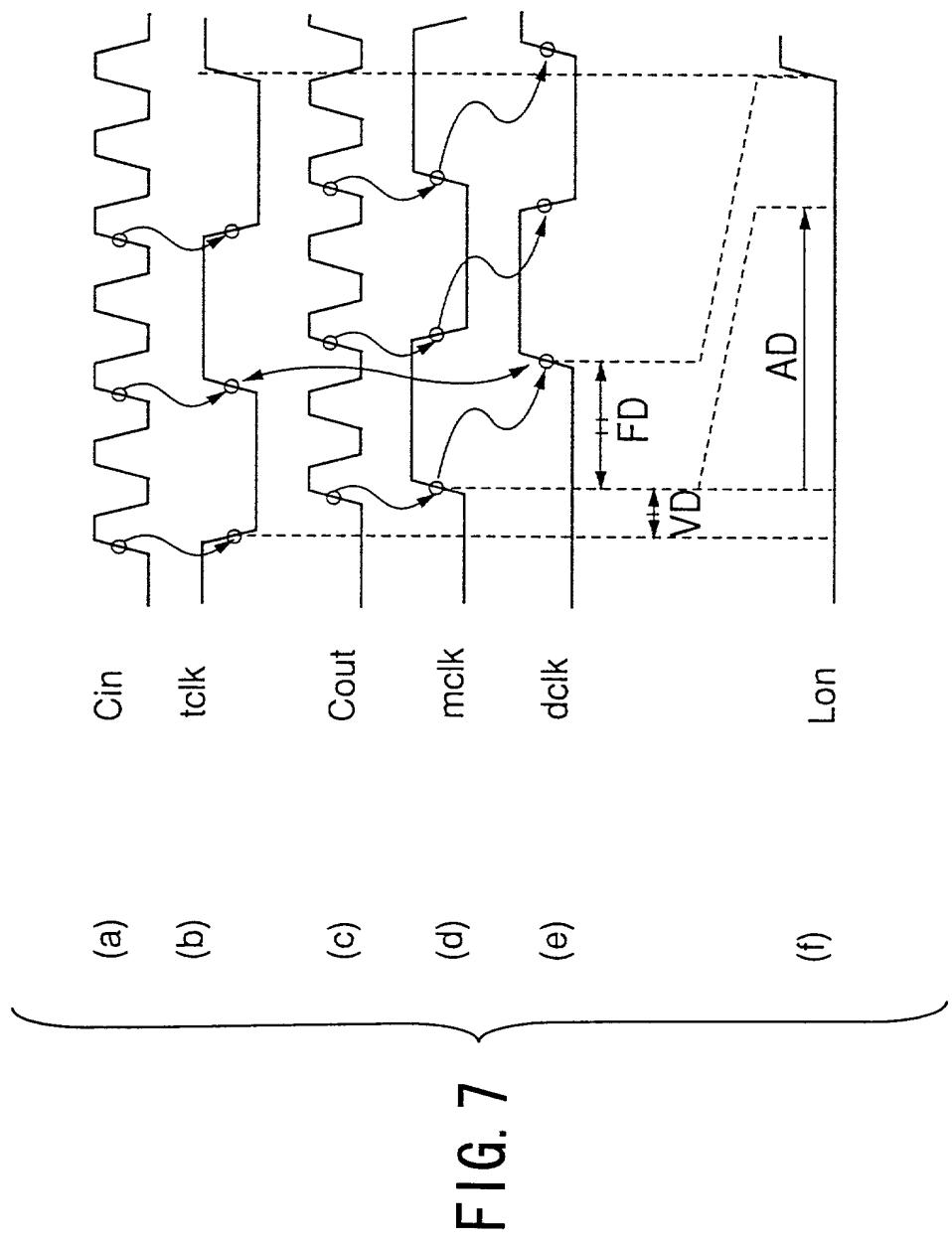


FIG. 8

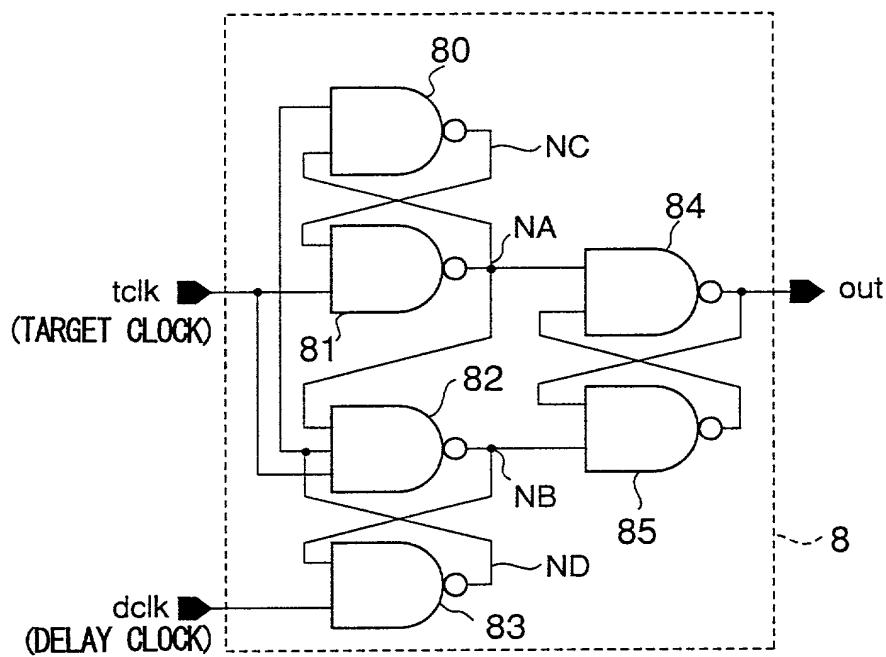


FIG. 9

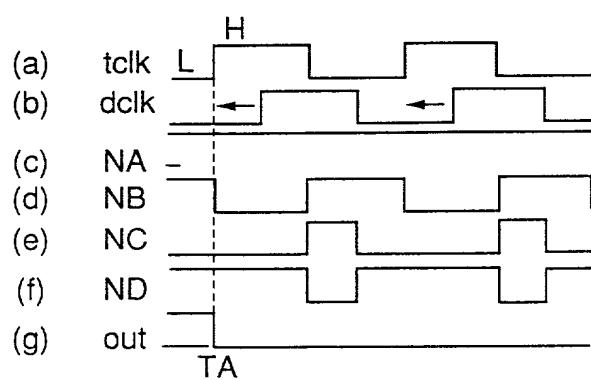


FIG. 10

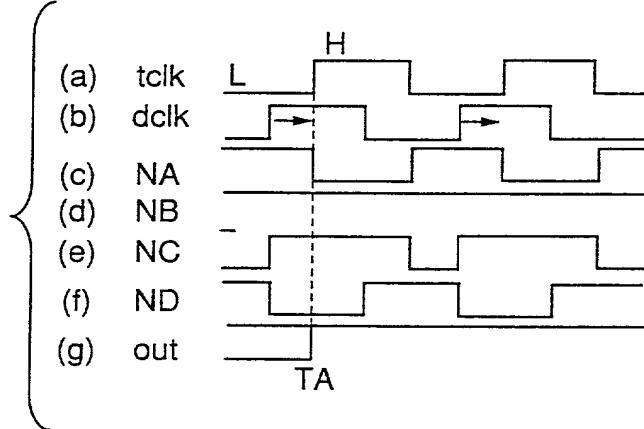


FIG. 1

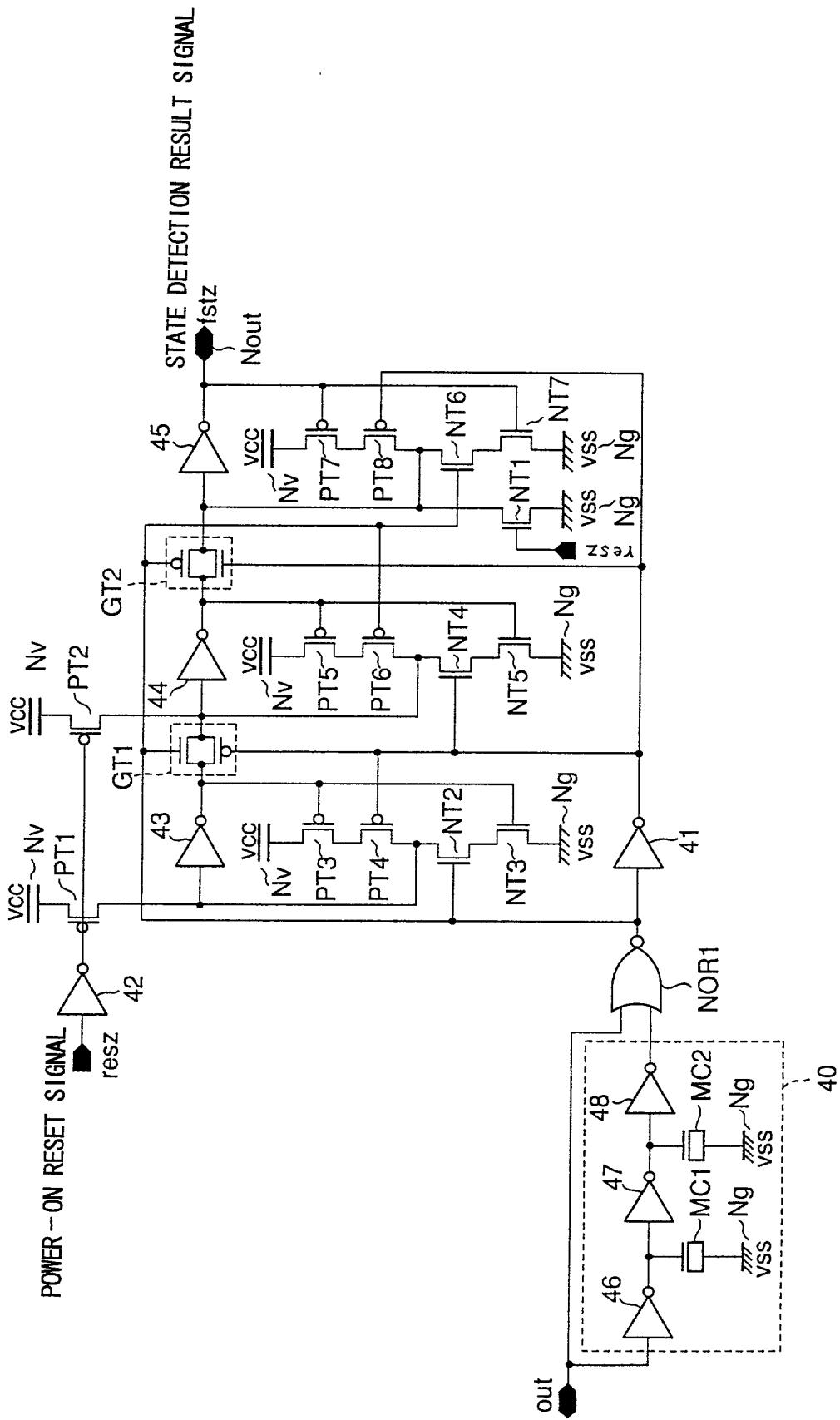


FIG. 12

